UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/940,792	08/29/2001	Paul A. Farrar	M4065.0382/P382-A	5268

24998 7590 03/14/2003

DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L STREET NW
WASHINGTON, DC 20037-1526

EXAMINER
LEE, EUGENE

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 03/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/940,792	Applicant(s) FARRAR ET AL.	
	Examiner Eugene Lee	Art Unit 2815	

-- The MAILING DATE of this communication appears on th cover sheet with the corr spondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 December 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *46-48 and 51-81* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *46-48 and 51-81* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 August 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, (1) a conductive path extending from said buried conductor pattern wherein said buried conductor pattern has a spherical pattern (claims 46-48); (2) at least one buried conductor pattern having a plate-shaped pattern, further comprising a second buried conductor pattern having a pipe-shaped pattern, further comprising a third buried conductor pattern having a spherical pattern (claim 74); at least two buried conductor patterns, wherein a first of said at least two buried conductor patterns is located below a second of said at least two buried conductor patterns and relative to a surface of said monocrystalline substrate, and a first conductive path extending from said first of said at least two buried conductor patterns and a second conductive path extending from said second of said at lest two buried conductor patterns, wherein said at least one of buried conductor patterns has a spherical pattern (claim 80) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to

> which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 46 thru 48 and 74 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Regarding claims 46-48, the specification does not describe at least one buried conductor pattern having a spherical pattern, and a conductive path extending from said buried conductor pattern.

Regarding claim 74, the specification does not describe at least one buried conductor pattern having a plate-shaped pattern, further comprising a second buried conductor pattern having a pipe-shaped pattern, further comprising a third buried conductor pattern having a spherical pattern.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 51 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 51 is dependent on cancelled claim 50. For the sake of compact prosecution, claim 51 will be interpreted as depending on claim 46, however, appropriate clarification and correction are required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 46, 52, 54, 56 thru 61, 72, and 75 are rejected under 35 U.S.C. 102(b) as being anticipated by Rostoker '768. Rostoker discloses (see, for example, FIG. 3) a semiconductor device comprising a monocrystalline substrate 4, and a plug of polysilicon (buried conductor pattern) 32. The plug of polysilicon contains indentations (plate–shaped pattern) 16. This plug of polysilicon also extends downward, forming a vertical structure (pipe-shaped pattern). Also, see FIG. 4 wherein Rostoker shows a plug of polysilicon 44 with a spherical pattern.

8. Claims 46, 52, 54 thru 61, 72 and 75 are rejected under 35 U.S.C. 102(b) as being anticipated by Lu et al. '581. Lu discloses (see, for example, FIG. 8) a semiconductor device comprising a single crystal silicon substrate 10, and a polysilicon layer (buried conductor pattern) 28. This polysilicon layer has a spherical, plate-shaped, and pipe-shaped pattern. An empty cavity 6 resides above the substrate.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 46 thru 48, 52, 61, 72 thru 75 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohtsuki 5,629,226 in view of Yamagata et al. '475. Ohtsuki discloses (see. for example, FIG .12) a substrate 1 comprising a polycrystalline silicon 13 and polycrystalline silicon layer (conductive pattern) 16. The polycrystalline silicon comprises three different patterns, a plate-shaped pattern at the top, a pipe-shaped pattern in the middle, and a spherical pattern at the bottom. Ohtsuki does not disclose the substrate as being monocrystalline. However, Yamagata discloses (see, for example, column 1, lines 52-54) that monocrystalline substrates have good controllability of crystal orientations and very less crystal defects. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use monocrystalline substrate in Ohtsuki's invention in order to have good controllability of crystal orientations and very less crystal defects.

11. Claims 46, 51, 52, 72 and 75 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. '789 in view of Yamagata et al. '475. Yamazaki discloses (see, for example, FIG. 4(C)and 5(C)) a semiconductor device comprising a silicon substrate 1, and metallic conductive layer (buried conductor pattern) 5. In column 4, lines 46-51, Yamazaki discloses the metallic conductive layer as being tungsten. Yamazaki does not disclose the substrate as being monocrystalline. However, Yamagata discloses (see, for example, column 1, lines 52-54) that monocrystalline substrates have good controllability of crystal orientations and very less crystal defects. Therefore it would have been obvious to one of ordinary skill in the art

at the time of invention to use monocrystalline substrate in Yamazaki's invention in order to have good controllability of crystal orientations and very less crystal defects.

12. Claims 72, 73, 75 thru 79 and 81 are rejected under 35 U.S.C. 103(a) as being unpatentable over Livengood et al. '454 B2 in view of Yamagata et al. '475. Livengood discloses (see, for example, FIG. 4) a semiconductor device comprising a substrate 402, substrate-vias (two buried conductor patterns) 440a/440d and interconnect lines (first and second conductive paths) 420a, 420c. In column 7, lines 28-32, Livengood states that additional substrate-vias may be provided. Witek does not disclose the substrate as being monocrystalline. However, Yamagata discloses (see, for example, column 1, lines 52-54) that monocrystalline substrates have good controllability of crystal orientations and very less crystal defects. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use monocrystalline substrate in Livengood's invention in order to have good controllability of crystal orientations and very less crystal defects.

13. Claims 62 thru 71 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rostoker '768 as applied to claims 46, 52, 54, 56 thru 61, 72, and 75 above, and further in view of Tsu et al. '420 B1. Rostoker does not disclose a processor system and a circuit coupled to said processor comprising a conductive structure. However, Tsu discloses (see, for example, FIG. 4C and FIG. 6) a memory array comprising a processor coupled to additional circuitry. In column 8, lines 61-*, Tsu states that the memory array may be embedded into a larger integrated circuit device wherein the memory array is included with control circuitry on the same integrated

circuit. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to include the semiconductor device of Rostoker into a memory array like Tsu in order to utilize Rostoker's device in memory circuits.

14. Claims 46, 47, 52, 75 thru 78, and 80 are rejected under 35 U.S.C. 103(a) as being unpatentable over Divakaruni et al. '686 B1 in view of Ohtsuki '226 in view of Yamagata et al. '475. Divakaruni discloses (see, for example, FIG. 4) a substrate 10 comprising trenches. One trench is extended deeper than the other trench. In FIG. 1, Divakaruni shows that multiple adjacent trenches may be formed in the substrate. In column 3, lines 13-17, Divakaruni discloses that the trenches are etched deeper than the adjacent trench. The trenches have spherical and pipe-shaped patterns. Divakaruni does not disclose the conductive patterns and conductive paths. However, Ohtsuki teaches (see, for example, column 4, lines 30-37 and FIG. 12) a polycrystalline silicon layer (conductive paths) 16 extending from a polycrystalline layer (conductor patterns) 13. The polycrystalline silicon layer and polycrystalline layer form a 1-transistor 1-capacitor memory cell. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to include the polycrystalline silicon layer and polycrystalline layer in Divakaruni's invention in order to form a 1-transistor 1-capacitor memory cell.

Divakaruni in view of Ohtsuki does not disclose the substrate as being monocrystalline. However, Yamagata discloses (see, for example, column 1, lines 52-54) that monocrystalline substrates have good controllability of crystal orientations and very less crystal defects. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention

to use monocrystalline substrate in order to have good controllability of crystal orientations and very less crystal defects.

Product-by-Process Limitations

15. While not objectionable, the Office reminds Applicant that "product by process" limitations in claims drawn to structure are directed to the product, per se, no matter how actually made. *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also, *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wethheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al.*, 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or *otherwise*. Note that applicant has the burden of proof in such cases, as the above case law makes clear. Thus, no patentable weight will be given to those process steps which do not add structural limitations to the final product.

For example, claims 56-61 and 62-71 contain the process limitation "at least one empty-spaced pattern in said substrate formed by annealing said substrate containing at least one hole drilled therein". Such a limitation merely recites a process of forming the buried conductor pattern and does not affect the final structural product. The presence of process limitations on product claims, which product does not otherwise patentably distinguish over prior art, can not impart patentability to the product.

Response to Arguments

16. Applicant's arguments with respect to claims 46-48, and 51-81 have been considered but are moot in view of the new ground(s) of rejection.

Regarding the Drawing Objection, none of the figures show a **conductive path** extending from said buried conductor pattern having a spherical pattern. FIG. 1f shows a spherical pattern, however, there is not a conductive path extending from the spherical pattern and the spherical pattern does not contain a buried conductor pattern, only empty space.

Regarding the applicant's argument that the trenches of Rostoker are formed by a different process than that of the applicant's trenches, see the ***Product-by-Process-Limitations*** paragraph above.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 703-305-5695. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 703-308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Eugene Lee

March 5, 2003

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800